(2 pts) Name:

AME 3623: Embedded Real-Time Systems

Midterm Exam

March 29, 2005

General instructions:

- This examination booklet has 9 pages.
- Do not forget to write your name at the top of the page and to sign your name below.
- The exam is closed book, closed notes, and closed electronic device. The exception is that you may have one page of your own notes.
- The exam is worth a total of 100 points (and 10% of your final grade).
- Explain your answers clearly and be concise. Do not write long essays (even if there is a lot of open space on the page). A question worth 5 points is only worth an answer that is at most 1.5 sentences.
- You have 1.25 hours to complete the exam. Be a smart test taker: if you get stuck on one problem go on to the next. Don't waste your time giving details that the question does not request. Points will be taken off for answers containing excessive, extraneous information.
- Show your work. Partial credit is possible, but only if you show intermediate steps.

Problem	Topic	Max	Grade
0	-	2	
1	Digital Logic	37	
2	Arithmetic	36	
3	Finite State Machines	25	
Total			

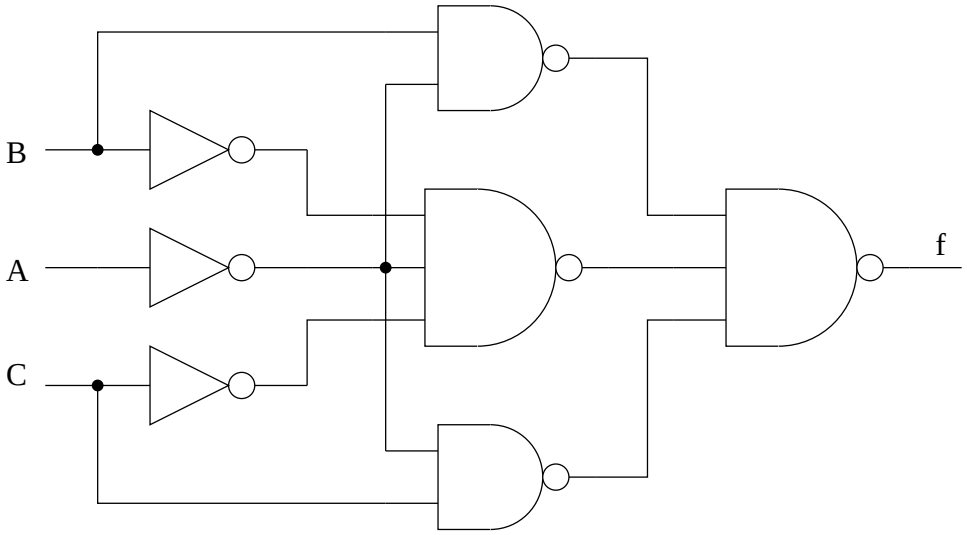
On my honor, I affirm that I have neither given nor received inappropriate aid in the completion of this exam.

Signature: _____

Date: _____

1. **Digital Logic** (37 pts)

Given the following circuit:



(a) (10 pts) Show the corresponding truth table.

(b) (7 pts) Give the Karnaugh map and show the clusters.

(c) (5 pts) What is the minimum algebraic description for f?

(d) (5 pts) Draw the corresponding circuit.

(e) (10 pts) (separate question) Using only 2-input NAND gates, design a 2-input XOR circuit.

2. **Arithmetic** (36 pts)

Given the following number in hexadecimal: $D3$. Assume that this is a two's complement, 8-bit number.

(a) (2 pts) What is the sign of this number?

(b) (5 pts) What is the decimal equivalent of this number?

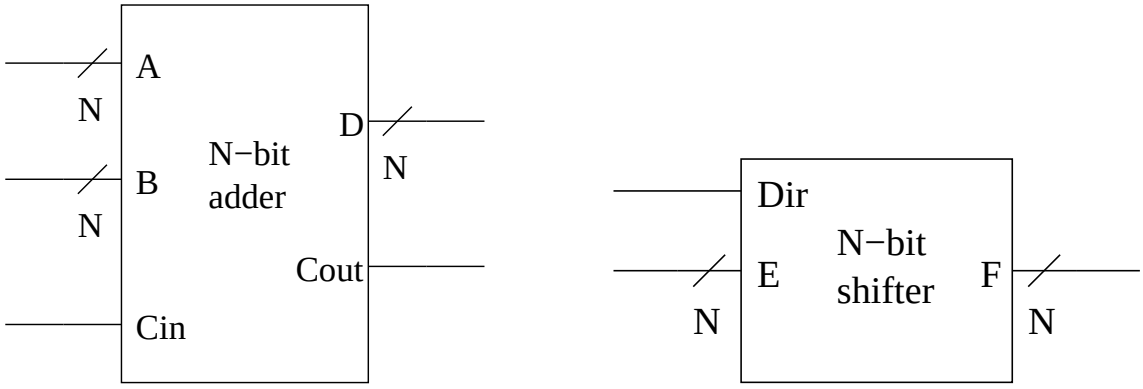
(separate question) Given two numbers (in decimal): $X = 19$ and $Y = 30$

(c) (9 pts) What are the binary equivalents of these numbers? Assume an 8-bit, twos complement representation.

(d) (5 pts) What is the additive inverse of Y?

(e) (5 pts) Subtract Y from X in binary (show your work)

(separate question) Given an N-bit adder device and an N-bit shifter device:



The N-bit adder takes three inputs A, B, and C_{in}, and produces two outputs D and C_{out}.

The N-bit shifter takes two inputs E and Dir, and produces an output F. When $Dir = 0$, the device shifts E to the right; when $Dir = 1$, the device shifts E to the left.

(f) (10 pts) Design a circuit that takes as input an N-bit number X and produces as output $X * 2.25$ (you may assume that you are working with unsigned binary).

3. **Finite State Machines** (25 pts)

Assume a 3-bit binary device that can execute the following operations on the downward edge of the clock:

- Decrement the number, and
- multiply the number by 2.

Assume a control bit that determines which operation will be performed. Design a Finite State Machine representation of this device using the following steps:

(a) (5 pts) What are the states?

(b) (5 pts) What are the events?

(c) (5 pts) What are the outputs?

(d) (10 pts) Show the full state transition diagram.