(2 pts) Name:

AME 3623: Embedded Real-Time Systems: Final Exam

May 13, 2005

- This examination booklet has 15 pages.
- Do not forget to write your name at the top of the page and to sign your name below.
- The exam is closed book, closed notes, and closed electronic device. The exception is that you may have one page of your own notes.
- The exam is worth a total of 200 points (and 20% of your final grade). You may "pass" on two of the 5 point questions (for which you will receive full credit). Make sure that you clearly indicate which questions you are passing on.
- Explain your answers clearly and be concise. Do not write long essays (even if there is a lot of open space on the page). A question worth 5 points is only worth an answer that is at most 1.5 sentences.
- You have 2 hours to complete the exam. Be a smart test taker: if you get stuck on one problem go on to the next. Don't waste your time giving details that the question does not request. Points will be taken off for answers containing extraneous information.
- Show your work. Partial credit is possible, but only if you show intermediate steps.

Problem	Topic	Max	Grade
0	-	2	
1	Logic	70	
2	Arithmetic	15	
3	Microprocessor Design	30	
4	Interrupts and I/O	33	
5	Serial Communication	30	
6	Finite State Machines	20	
7	Bonus	2	
Total		202	

On my honor, I affirm that I have neither given nor received inappropriate aid in the completion of this exam.

Signature: _____

Date: _____

1. **Logic** (70 pts)

Given the following function:

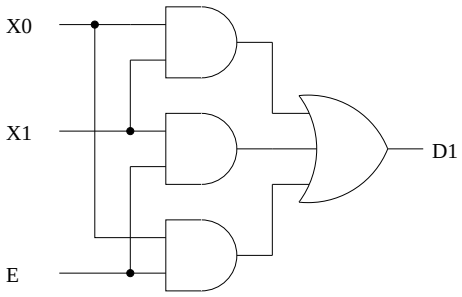
A	B	C	D	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

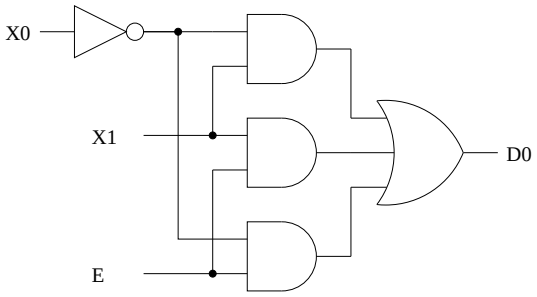
(a) (10 pts) Show the Karnaugh map and the clusters.

(b) (7 pts) What is the algebraic expression for the corresponding circuit?

(c) (7 pts) Show the circuit

Given the following circuits:

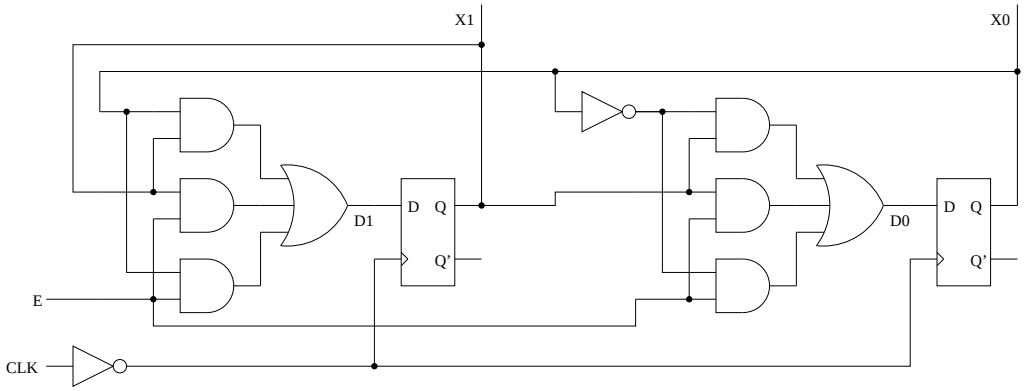




(d) (15 pts) Show the corresponding truth table for $D0$ and $D1$.

E	$X1$	$X0$	$D1$	$D0$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Given the following sequential logic circuit (note its relationship to the circuits in the previous problem):



(e) (8 pts) Assume an initial condition of $X1 = 0$ $X0 = 1$, and that $E = 1$. Show the timing diagram for 4 clock cycles (include $X1$, $X0$ and CLK).

(f) (8 pts) Assume an initial condition of $X1 = 1$ $X0 = 1$, and that $E = 0$. Show the timing diagram for 4 clock cycles (include $X1$, $X0$ and CLK).

(g) (5 pts) From the perspective of a Finite State Machine representation of this circuit, what are the events/inputs?

(h) (10 pts) Show the state transition diagram.

2. **Arithmetic** (15 pts)

Consider the following decimal numbers: $X = 38$ and $Y = 47$

(a) (7 pts) What is the two's complement binary representation of $-Y$ (assume an 8 bit representation)?

(b) (8 pts) In binary, subtract Y from X (show your work).

3. **Microprocessor Design** (30 pts)

(a) (5 pts) What is the function of the ALU?

(b) (5 pts) What is the function of the program counter?

(c) (10 pts) Give two examples of signals generated by the instruction decoder.

(d) (5 pts) Explain (in brief) the function of the "chip select" signal in a memory circuit.

(e) (5 pts) Explain (in brief) the function of the clock signal in a memory circuit.

4. **Interrupts and I/O** (33 pts)

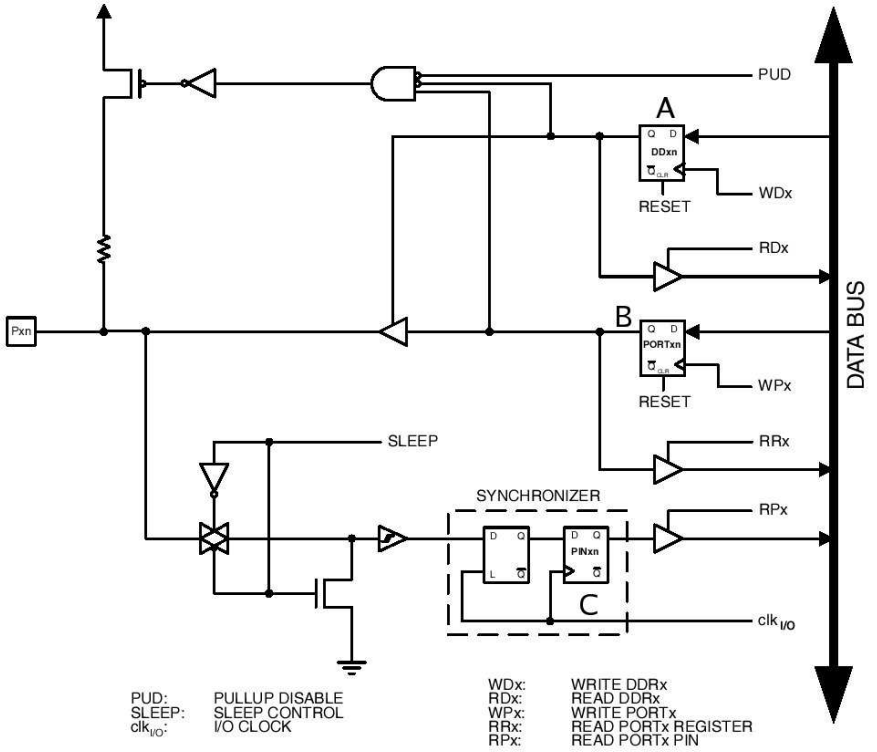
(a) (5 pts) True/false: in pulse-width modulation control, information is encoded in the frequency of the signal.

(b) (7 pts) For the given clock rate and prescaler configuration of the mega8 timer0, give the time (in microseconds) between timer increments (reduced fractions are fine, where necessary).

Prescaler	1 MHz clock	16 MHz clock
No prescaler		
Div 8		
Div 64		
Div 256		
Div 1024		

(c) (5 pts) Assume that we configure timer0 so that it uses a prescaler of 64 and produces an interrupt. Also assume a clock frequency of 16MHz. How often will an interrupt be generated?

Consider the diagram for PORT B bit 2 (the 3rd bit):



(d) (8 pts) What effect does the following code have on the state of this circuit (in terms of flip-flop state)? What effect does this state change have?

```
DDRB &= 4;
```

(e) (8 pts) What effect does the following code have on the state of this circuit (in terms of flip-flop state)? What effect does this state change have?

```
PORTB &= 0xFB;
```

5. **Serial Communication** (30 pts)

(a) (10 pts) Explain why we do not use a start bit value of "1" in our infrared serial implementation.

(b) (5 pts) Does the receiver or the sender compute the checksum value?

(c) (5 pts) True/False: a UART can perform byte-level error correction and detection.

(d) (5 pts) True/False: a UART can perform packet-level error correction and detection.

(e) (5 pts)

Consider a packet that contains the following values: $0x45, 0x12, 0xFA$. What is the checksum value?

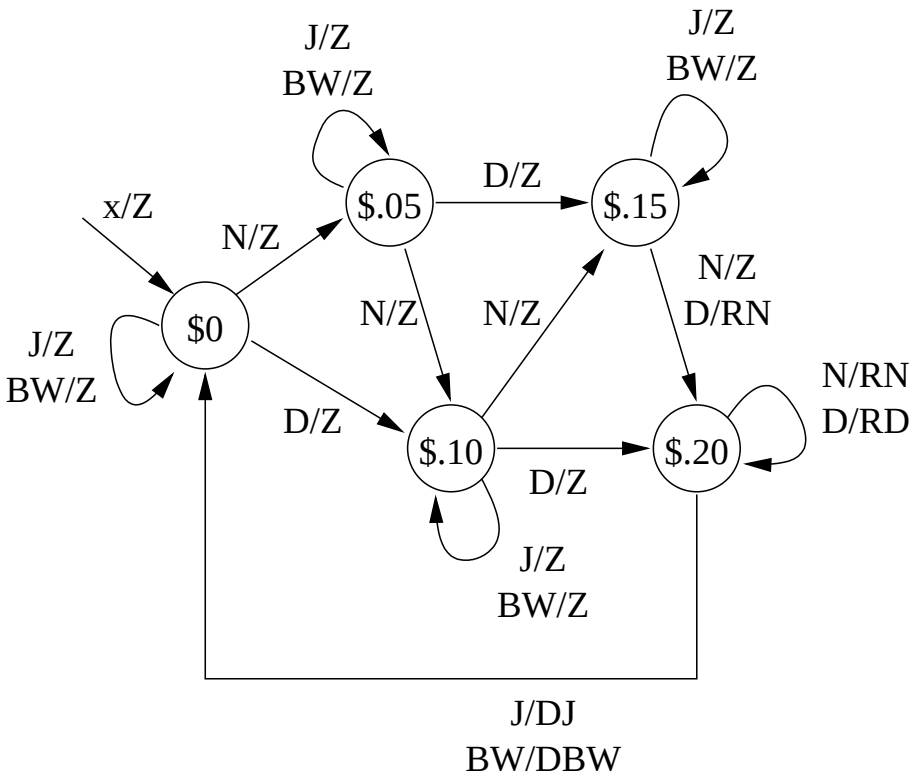
6. **Bonus** (2 pts)

What is the magic number?

7. **Finite State Machines** (20 pts)

Below is the state transition diagram of the vending machine that we designed in class. Recall that once the machine receives \$.20 (composed of nickels and dimes), it will respond to a button press by dispensing the requested drink (Jolt or Buzz Water). Redesign this FSM to add the following "Easter Egg" feature:

Starting from the \$0 state, if the user inserts the following coins in this specific order: nickel, dime, nickel, the machine immediately returns the three coins and is ready to dispense a drink and an additional nickel.



Where the events are: N = Nickel (insertion); D = Dime (insertion); J = Jolt (request); BW = Buzz Water (request).

And the actions are: RN = Return Nickel; RD = Return Dime; DJ = Dispense Jolt; DBW = Dispense Buzz Water; Z = no action.

Hint: in order to implement the Easter Egg feature, you will need to add additional states and state transitions.

(a) (5 pts) What are the states in this new FSM?

(b) (5 pts) What are the actions in this new FSM?

(c) (10 pts) Show the state transition diagram (if you choose, you may modify the diagram on the previous page).