Embedded Real-Time Systems (AME 3623)
Homework 3

April 22, 2005

This homework assignment is due on Monday, May 2nd at 5:00pm. It must be handed in by hand or using the blackboard digital dropbox (use the "send file" option) in either postscript or pdf format.

This assignment must be done individually: do not share your answers with others or look at the answers of others.

Question 1

1. Describe (in brief) the function of the status register.

2. Describe the similarities and differences between the Atmel Mega8 RAM and its general purpose registers.

Question 2

1. Name the four distinct components that **can** compose a serial data frame. Describe the function of each.

2. Name the three levels of serial processing. Describe in brief the approach to preventing and/or detecting errors at each of these levels.

Question 3

1. Given a ROM module made up of 2048 bytes. How many input lines are necessary? List them.

Question 4

The OUmel mega8 processor has a similar architecture as the Atmel mega8. It supports a set of instructions that are encoded as follows:

Assembly	Description	Machine code
AND	bit-wise AND	0 0 1 0 0 0 r d d d d d r r r r
ADD	add with carry	0 0 0 0 1 1 r d d d d d r r r r
INC	increment	1 0 0 1 0 1 0 d d d d d 0 0 1 1
SWAP	swap nybbles	1 0 0 1 0 1 0 d d d d d 0 0 1 0

Assume the bits are arranged with the most significant bit (I15) on the left.

Assume an arithmetic logical unit with two control bits ($C1$ and $C0$). Assume the following bit combinations for the following operations:

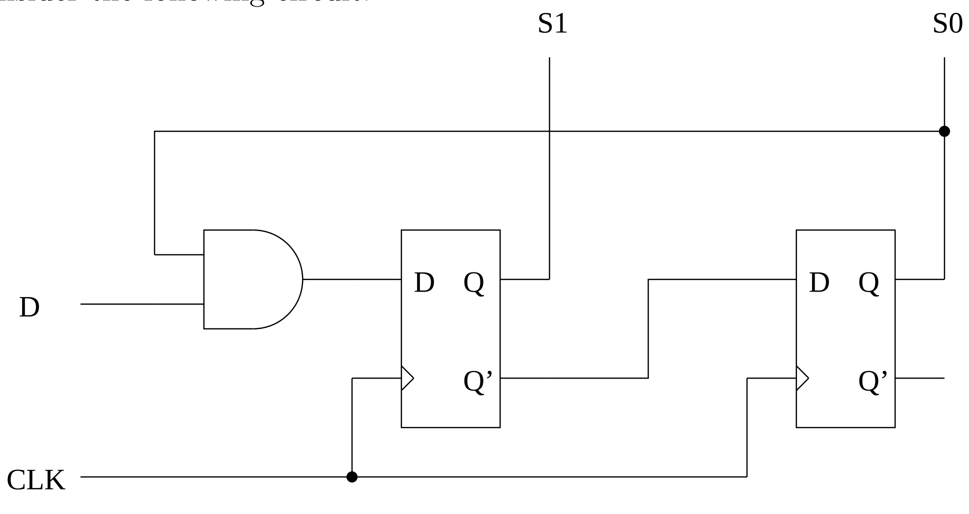
C1	C0	Operation
0	0	AND
0	1	ADD
1	0	INC
1	1	SWAP

1. Give the algebraic expression for the circuit that uniquely identifies each of the four instructions.

2. Show the circuit that takes as input $I15...I0$ and produces the bits $C1$ and $C0$ for input into the ALU.

Question 5

Consider the following circuit:



1. Assume $D = 1$ and an initial condition of $S1 = 0$ and $S0 = 0$. Show the timing diagram for 5 complete clock cycles.

2. Assume $D = 0$ and an initial condition of $S1 = 1$ and $S0 = 0$. Show the timing diagram for 5 complete clock cycles.

Consider the finite state machine representation of this circuit.

3. What are the states?

4. What are the events?

5. Show the corresponding state transition diagram.

Question 6

1. What two conditions must be met for us to have a “shared data problem?”

2. What are the advantages and disadvantages of polling over interrupts.