(2 pts) Name:

AME 3623: Embedded Real-Time Systems

Midterm Exam

Solution Set

March 9, 2006

Problem	Topic	Max	Grade
0	-	2	
1	Digital Logic	32	
2	Number Systems	15	
3	Sequential Logic and Finite State Machines	20	
4	Memory	15	
5	Microcontroller I/O	18	
Total			

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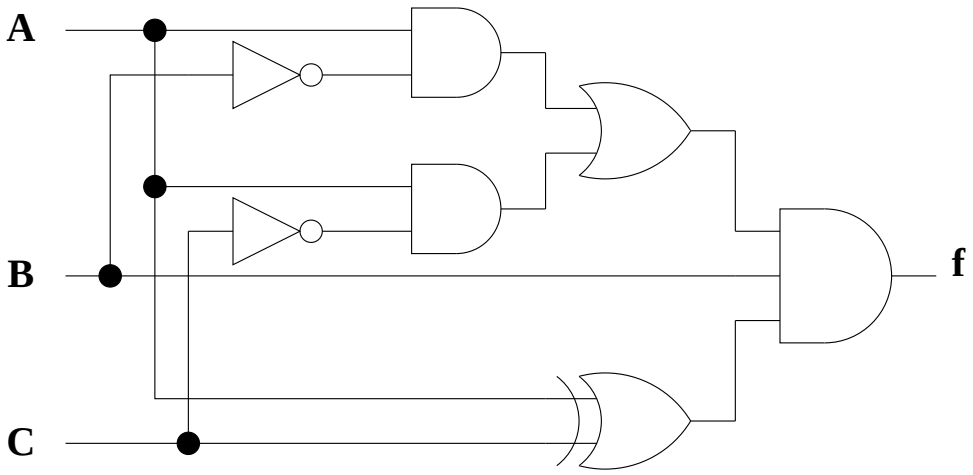
1. **Digital Logic** (32 pts)

Given the following circuit:



(a) (10 pts) Show the corresponding truth table.

A	B	C	f
0	*0*	*0*	*0*
0	*0*	*1*	*0*
0	*1*	*0*	*0*
0	*1*	*1*	*0*
1	*0*	*0*	*0*
1	*0*	*1*	*0*
1	*1*	*0*	*1*
1	*1*	*1*	*0*

Observations: $B = 0$ *implies that* $f = 0$. *When* $B = 1$, *the top-most AND gate output is* 0. $A = C$ *implies that* $f = 0$.

Given the following truth table:

A	B	C	D	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(b) (7 pts) Give the Karnaugh map and show the clusters.

CD \ AB	00	01	11	10
00	1	1	0	0
01	1	1	0	1
11	0	1	0	0
10	0	1	0	0

(A = columns, B = columns, C = rows, D = rows)

(c) (5 pts) What is the corresponding algebraic description for f (that comes directly from the clusters)?

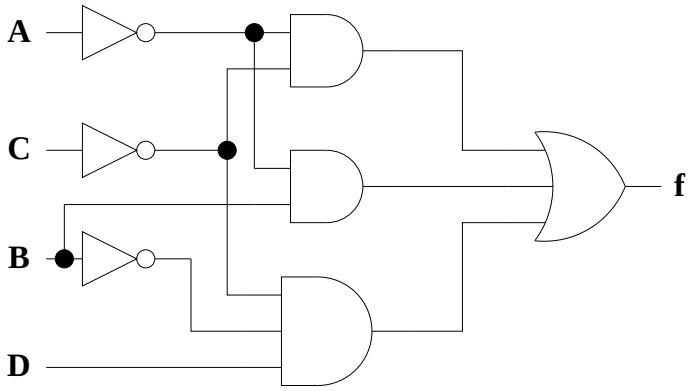
$f = \overline{A}\,\overline{C} + \overline{A}B + \overline{B}\,\overline{C}D$

(d) (5 pts) Give a simplified algebraic description for f

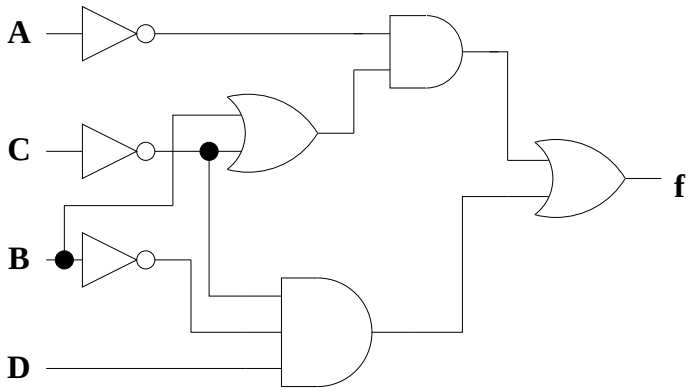
$f = \overline{A}(\overline{C} + B) + \overline{B}\,\overline{C}D$
or
$f = \overline{A}B + \overline{C}\,(\overline{A} + \overline{B}\,D)$

(e) (5 pts) Draw the corresponding circuit.

here is the unsimplified circuit:



And a simplified one:



2. **Number Systems** (15 pts)

Given the following number in hexadecimal: $A1$.

(a) (5 pts) What is the binary equivalent of this number?

$0xA5 = 10100001$

(b) (5 pts) What is the decimal equivalent of this number?

The decimal equivalent of this is: $128 + 32 + 1 = 161$

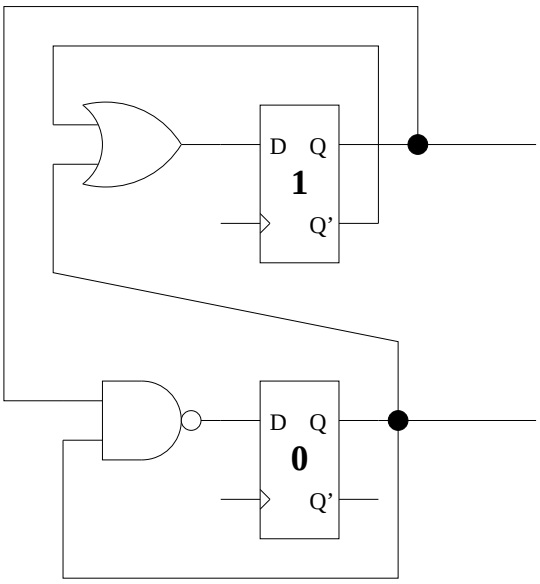
(separate question) Given the decimal number 67:

(c) (5 pts) What is the binary equivalent of this number? (show your work)

value	**binary**	i	2^i
67	*0000000*		
		6	*64*
3	*1000000*		
		1	*2*
1	*1000010*		
		0	*1*
0	*1000011*		

3. **Sequential Logic** (20 pts)

Given the following circuit:



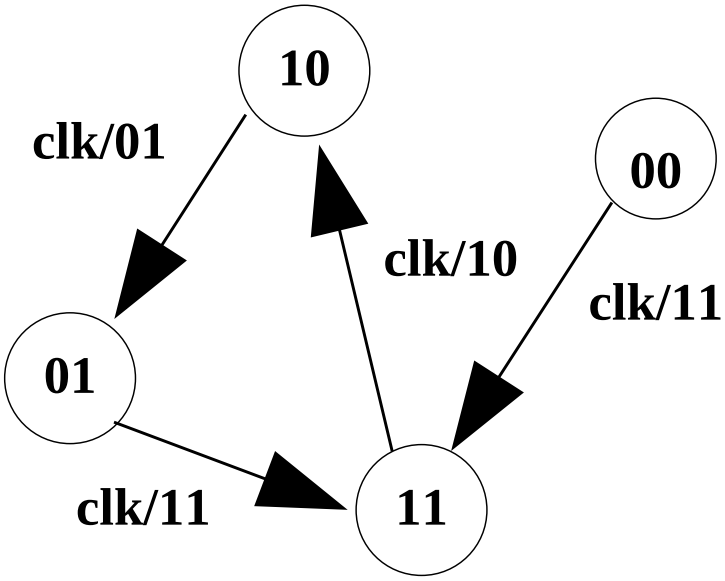
(a) (5 pts) What are the possible states (list all of them)?

All combinations of the individual bit values (there are 4 in total):
$00, 01, 10, 11$

(b) (10 pts) Assume an initial state of $Q1 = 0$ and $Q0 = 1$. What is the sequence of states over 5 clock cycles?

01, 11, 10, 01, 11, 10

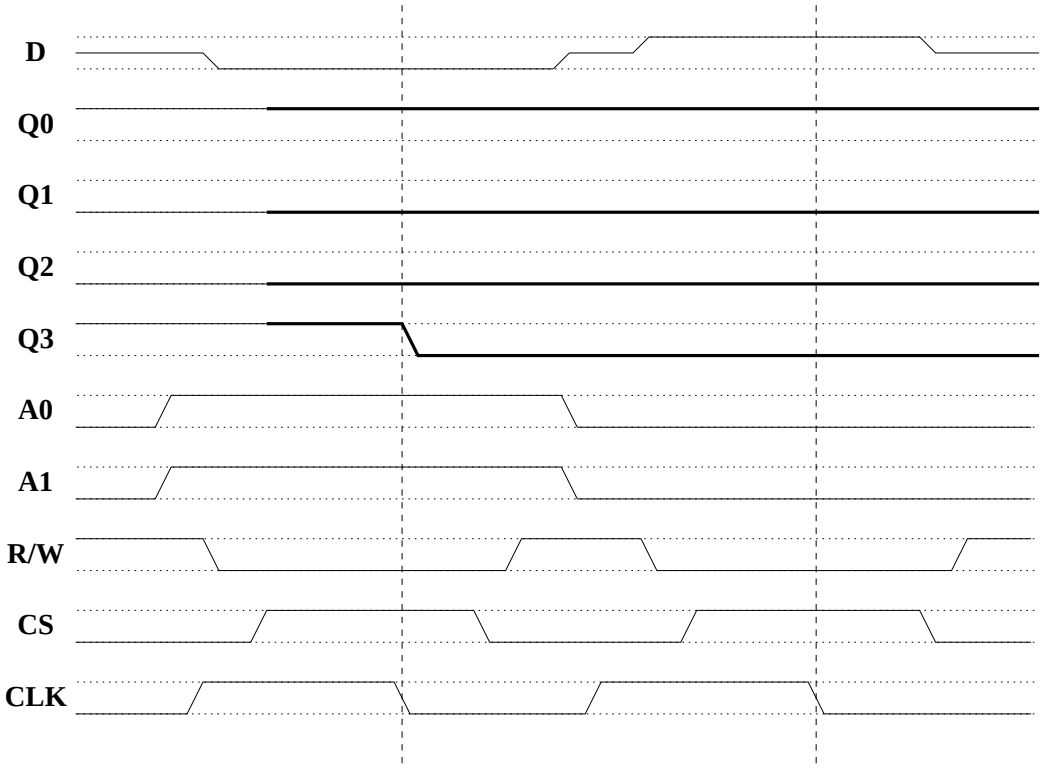
(c) (5 pts) Draw the finite state machine representation of this circuit.



(In this case, I will accept your answer if you did not place the output labels on the transitions).

4. **Memory** (15 pts)

(a) (15 pts) For the timing diagram below, fill in the missing traces.

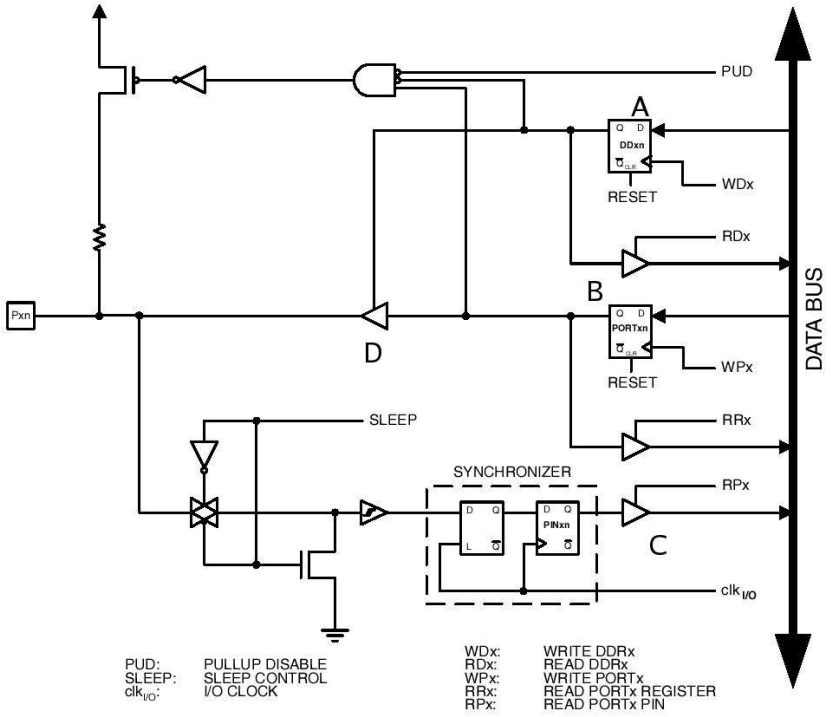


Both memory operations are write operations (to elements 3 and 0, respectively). Note, however, that the state of Q0 does not change (it was already in a state of "1").

(b) (5 pts) Explain in brief the function of the address signals (in general).

A memory chip is composed of many individual memory elements, arranged as a long array. The address signals tell us which element is being written to or read from during an operation. (note that for N address signals, we have 2^N memory elements).

5. **Microcontroller I/O** (18 pts)



(a) (8 pts) Identify component "A". Explain in brief the function of this type of component (in general, not in this circuit).

Component "A" is a D-type flip-flop, which stores one bit of information. The value that is stored is output through Q (the inverted value is $\overline{Q}$). When the clock input transitions from high to low, the data input (D) is stored.

(b) (10 pts) What effect does the following code have on the state of this circuit (in terms of components A, B, C, and D)? State any assumptions that you must make.

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DDRB = DDRB | 0x10;
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This line of code ensures that bit 4 (counting from 0) of the DDRB register is set to 1. So - after the code is executed, flip-flop A will be in a state of 1 (for bit 4 of port B only; all other DDRx bits will remain unchanged). This has the effect of ensuring that the select line of component D (a tristate buffer) will be high. This means that the pin will be an output pin (i.e., it will be driven high or low, depending on the state of flip-flop B).
Components B and C do not change state as a result of executing this code.