Embedded Real-Time Systems (AME 3623)
Homework 3 Solutions

February 24, 2006

Question 1

1. (5pts) Given the binary number: 1001011. What is the decimal equivalent? Show your work.

   $64 + 8 + 2 + 1 = 75$

2. (5pts) Given the binary number: 111010. What is the decimal equivalent? Show your work.

   $32 + 16 + 8 + 2 = 58$

3. (5pts) Given the decimal number: 68. What is the binary equivalent? Show your work (all of the steps of the algorithm that we discussed in class).

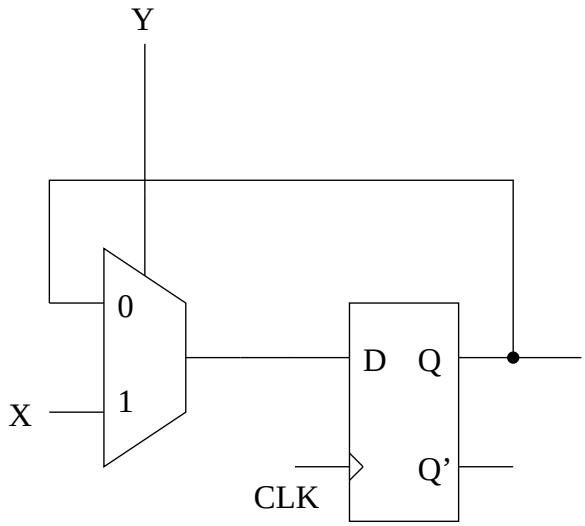
value	**binary**	i	2^i
68	0000000		
		6	64
4	1000000		
		2	4
0	1000100		

4. (5pts) Given the decimal number: 122. What is the binary equivalent? Show your work.

value	**binary**	i	2^i
122	0000000		
		6	64
58	1000000		
		5	32
26	1100000		
		4	16
10	1110000		
		3	8
2	1111000		
		1	2
0	1111010		

Question 2

Given the following circuit:



(15pts) Explain in detail what this circuit does in terms of its inputs (X, Y, and CLK). (Multiplexer notation note: the 0 and 1 tell you which input is selected when Y is in these states)

When $Y = 0$, the flip-flop will maintain its current state (even as the clock cycles).

When $Y = 1$, the flip-flop stores the value of X when the clock transitions from high to low.

(Note: this is going to become a critical component in the design of our RAM)

Question 3

Following the steps below (and our design procedure from class), design a counter that counts down from 7 to 2. After 2, the counter returns to 7.

1. (10pts) Show the truth table

   Our general approach will be to use D flip-flops with a common clock signal driving each one. So – we are looking to design a combinatorial circuit that will transform the set of Qi's (representing the current state) into a representation of the next state (the Di's). In addition, since the 000 and 001 cases never occur, we can treat these as "don't care" conditions.

Q2	Q1	Q0	D2	D1	D0
0	0	0	x	x	x
0	0	1	x	x	x
0	1	0	1	1	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

2. (15pts) Show the Karnaugh map for the first bit, the clusters, and the resulting algebraic expression.

$D0$

		Q2			
	$Q2Q1$	Q1			
$Q0$		00	01	11	10
	0	x	1	1	1
$Q0$					
	1	x	0	0	0

$D0 = \overline{Q0}$

3. (15pts) Show the Karnaugh map for the second bit, the clusters, and the resulting algebraic expression.

$D1$

		Q2			
	$Q2Q1$	Q1			
$Q0$		00	01	11	10
	0	x	1	0	1
$Q0$					
	1	x	1	1	0

$D1 = \overline{Q0}\,\overline{Q1} + Q0Q1 + Q1\overline{Q2} = \overline{Q0 \oplus Q1} + Q1\overline{Q2} = \overline{Q0} \oplus Q1 + Q1\overline{Q2}$

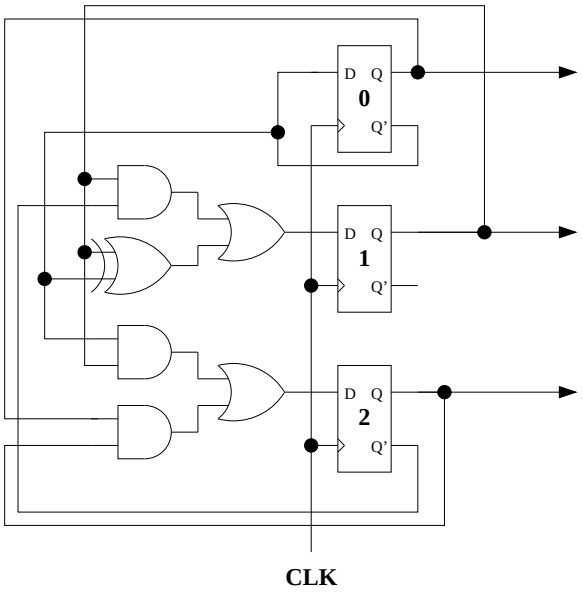
4. (15pts) Show the Karnaugh map for the third bit, the clusters, and the resulting algebraic expression.

   $D2$

$Q2Q1$ \ $Q0$		Q2 Q1 00	01	11	10
$Q0$	0	x	1	1	0
	1	x	0	1	1

   $D2 = \overline{Q0}\ Q1 + Q0Q2$

5. (15pts) Show the full circuit



Question 4

How much time did you spend on this assignment?