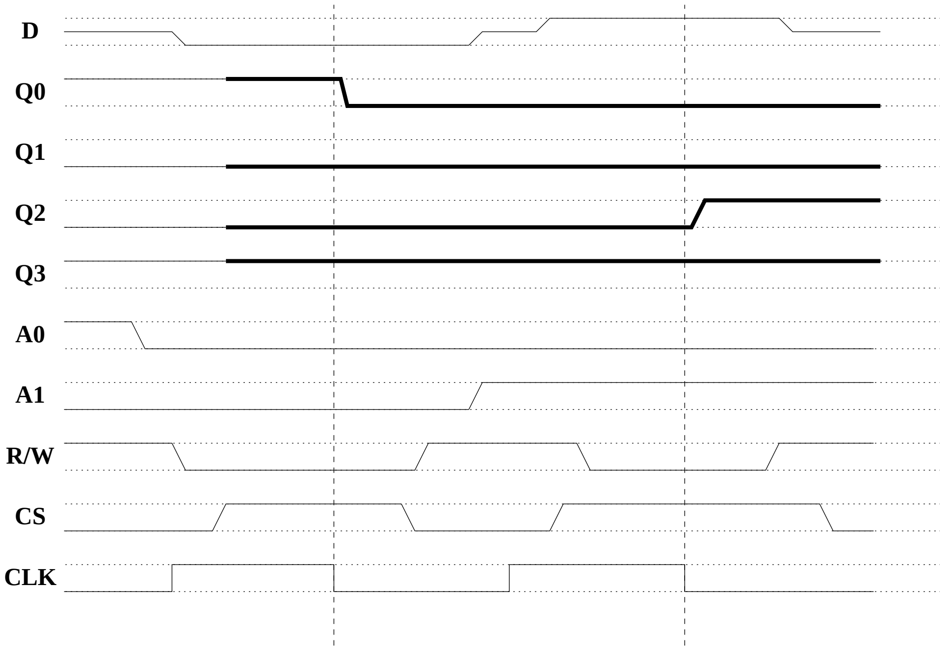
Embedded Real-Time Systems (AME 3623)
Homework 4 Solutions

February 28, 2006

Question 1

(10pts) Consider the four-element memory "chip" that we discussed in class. Given the following timing diagram, fill in the missing traces ($Q0$, $Q1$, $Q2$, and $Q3$).

Both memory accesses are write operations; they affect the state of Q0 and Q2 (but only when the clock transitions from high to low).

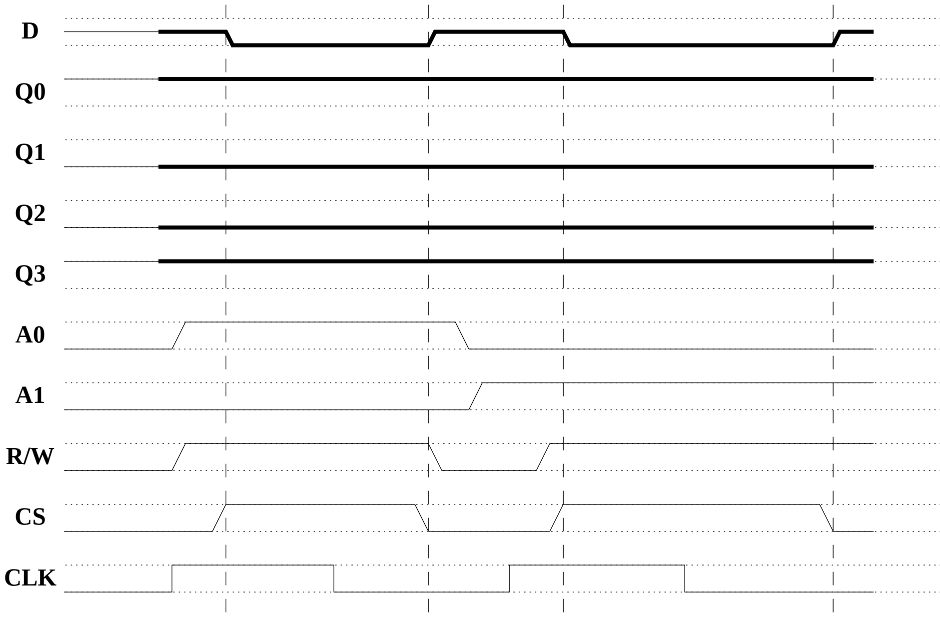


(answer is shown in bold)

Question 2

(10pts) Consider the same four-element memory chip. Given the following timing diagram, fill in the missing traces (D, $Q0$, $Q1$, $Q2$, and $Q3$).

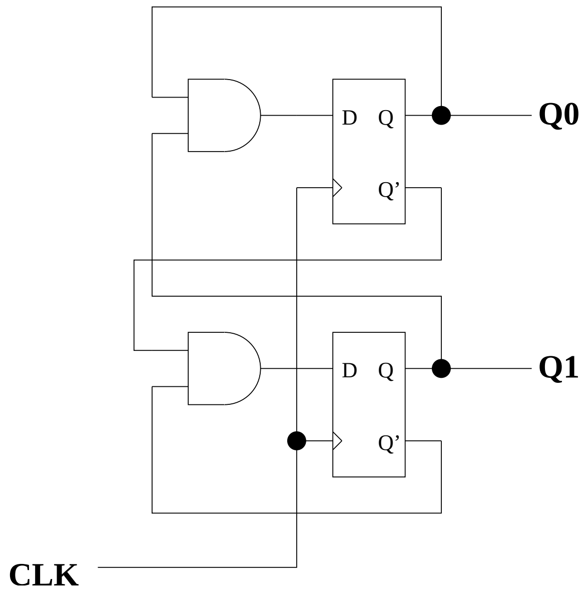
Both of these operations are read operations of elements Q1 and Q2. None of the memory elements change state. The data bus is driven during the entire time that the chip select line is high.



(answer is shown in bold)

Question 3

Consider the following circuit:



1. (5pts) List all possible states that this circuit can be in (the possible combinations of $Q1$ and $Q0$).

   The four possible states are : Q1/Q0 = 00, 01, 10, and 11.

2. (10pts) Assume an initial state of $Q1 = 1$ and $Q0 = 1$. List the sequence of states given six clock cycles (6 high-low transitions).

time	*Q1*	*Q0*	*D1*	*D0*
0	*1*	*1*	*0*	*1*
1	*0*	*1*	*0*	*0*
2	*0*	*0*	*1*	*0*
3	*1*	*0*	*0*	*0*
4	*0*	*0*	*1*	*0*
5	*1*	*0*	*0*	*0*
6	*0*	*0*	*1*	*0*

(note that this is **NOT** *a truth table)*

Question 4

(10pts) Is the “chip select” signal for a memory chip an input or an output (with respect to the chip)? Explain in brief its function.

The chip select signal is an input into a memory chip. It informs the chip that it is about to be involved in a read or a write operation. This is a necessary signal because we typically have many devices (including memory chips) that are connected to the same data bus.

Question 5

How much time did you spend on this assignment?