Embedded Real-Time Systems (AME 3623)
Homework 3

February 27, 2007

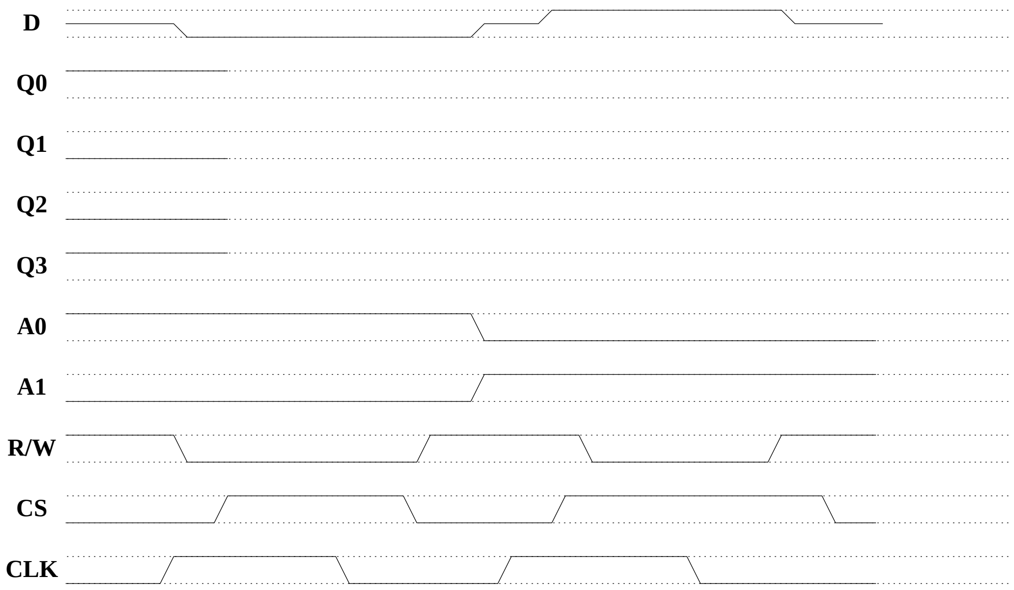
This homework assignment is due on Thursday, March 8th at 5:00pm. Your work may be handed in electronically (use the **Homework 3** digital dropbox on D2L) or in hardcopy form (in person or in office).

This assignment must be done individually: do not share/discuss your answers with others or look at the answers of others.

Question 1

(10pts) Consider the four-element memory "chip" that we discussed in class (each element is "one bit wide"). Given the following timing diagram, fill in the missing traces ($Q0$, $Q1$, $Q2$, and $Q3$).

Hint: first re-examine the rules for writing to and reading from a memory chip.

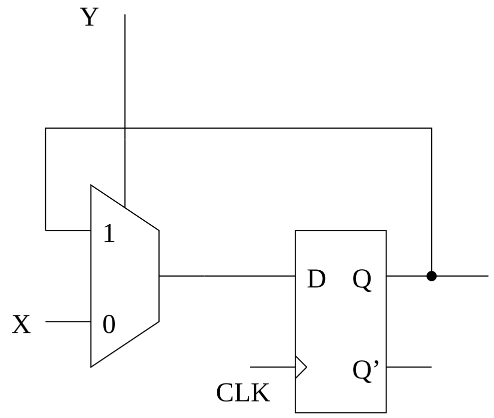


Question 2

(10pts) Consider the same four-element memory chip. Given the following timing diagram, fill in the missing traces (D, $Q0$, $Q1$, $Q2$, and $Q3$).

Question 3

Consider the following circuit:



1. (10pts) Describe the behavior of this component of a memory circuit in terms of the inputs X, Y, and CLK. Specifically, describe what Q does as these signals change.

2. (10pts) Assume memory control signals in the previous problems (CS, R/W, $A1$, and $A0$), and that this is memory element number 2 (counting from 0). Give the truth table for Y given these input signals such that this memory element is written to at the appropriate time.

CS	R/W	$A1$	$A0$	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

3. (10pts) Give the truth table for $\bar{Y}$.

CS	R/W	$A1$	$A0$	$\bar{Y}$
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

4. (10pts) Using what you know about $\bar{Y}$, design the circuit that implements Y.