Embedded Real-Time Systems (AME 3623)
Homework 3 Solutions

March 9, 2007

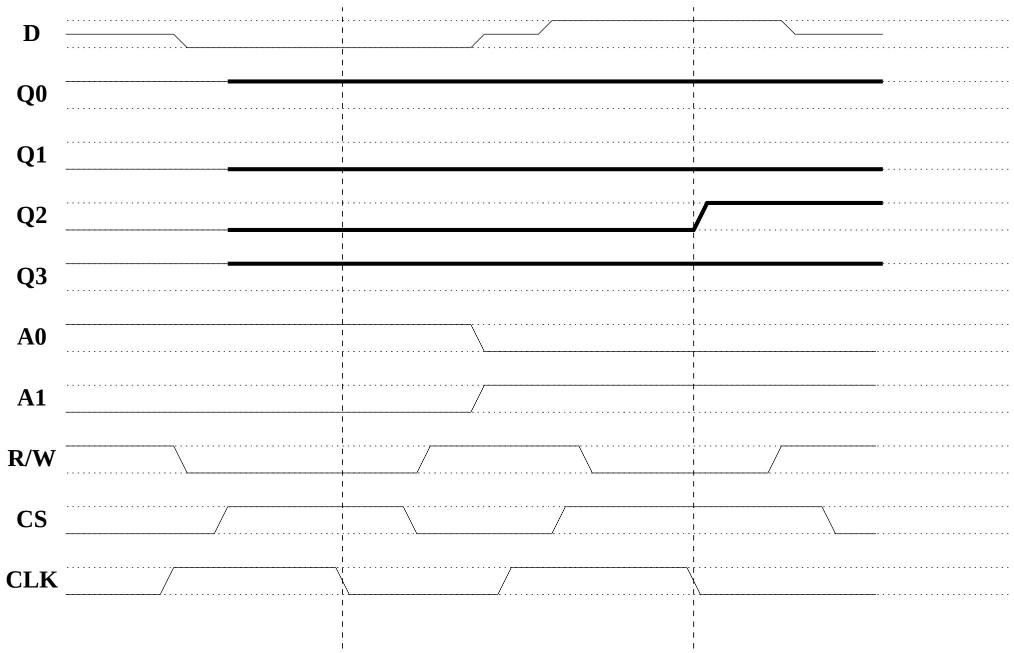
Question 1

(10pts) Consider the four-element memory "chip" that we discussed in class (each element is "one bit wide"). Given the following timing diagram, fill in the missing traces ($Q0$, $Q1$, $Q2$, and $Q3$).

Hint: first re-examine the rules for writing to and reading from a memory chip.

Both memory accesses are write operations; they affect the state of Q1 and Q2, respectively (but only when the clock transitions from high to low). However, the state of Q1 does not change.

(answer is shown in bold)

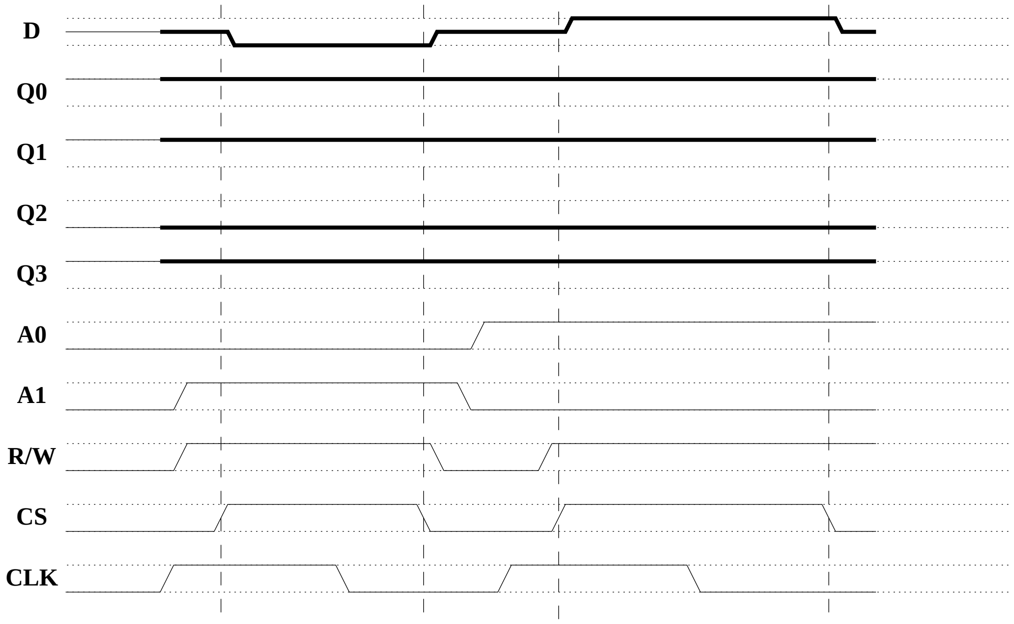


Question 2

(10pts) Consider the same four-element memory chip. Given the following timing diagram, fill in the missing traces (D, $Q0$, $Q1$, $Q2$, and $Q3$).

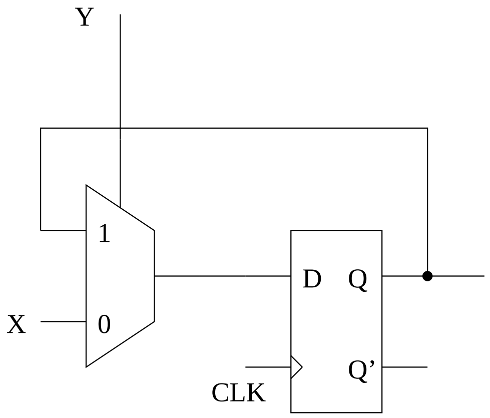
Both of these operations are read operations of elements Q2 and Q1. None of the memory elements change state. The data bus is driven during the entire time that the chip select line is high.

(answer is shown in bold)



Question 3

Consider the following circuit:



1. (10pts) Describe the behavior of this component of a memory circuit in terms of the inputs X, Y, and CLK. Specifically, describe what Q does as these signals change.

   When $Y = 1$, Q never changes state no matter what X and CLK do.

   When $Y = 0$, Q copies the value of X when CLK transitions from high to low. In this case, we can say that X is written to this memory component.

2. (10pts) Assume memory control signals in the previous problems (CS, R/W, $A1$, and $A0$), and that this is memory element number 2 (counting from 0). Give the truth table for Y given these input signals such that this memory element is written to at the appropriate time.

CS	R/W	$A1$	$A0$	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

3. (10pts) Give the truth table for $\bar{Y}$.

CS	R/W	$A1$	$A0$	$\bar{Y}$
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4. (10pts) Using what you know about $\bar{Y}$, design the circuit that implements Y.