0. Name (2 pts):

AME 3623: Embedded Real-Time Systems

Midterm Exam

Solution Set

March 13, 2008

Problem	Topic	Max	Grade
0	Name	2	
1	Digital Logic	27	
2	Sequential Logic	17	
3	Memory	20	
4	Microcontrollers	20	
5	Timers	16	
Total			

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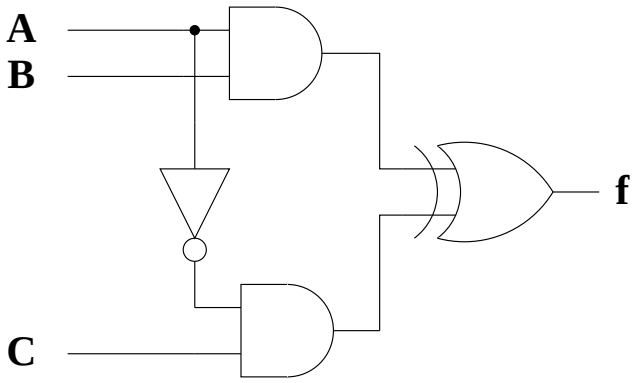
1. **Digital Logic** (27 pts)

Given the following circuit:



(a) (8 pts) Show the corresponding truth table.

A	B	C	f
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*1*
1	*0*	*0*	*0*
1	*0*	*1*	*0*
1	*1*	*0*	*1*
1	*1*	*1*	*1*

Given the following truth table:

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

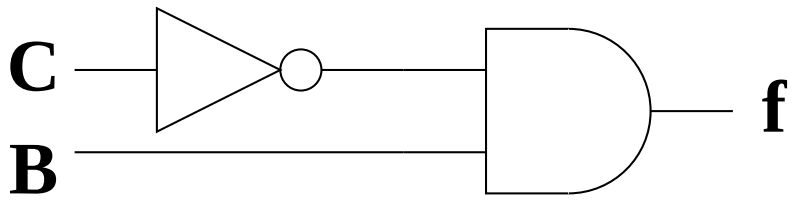
(b) (5 pts) Give the "minterm" form of the corresponding algebraic expression.

$f = \bar{A}B\bar{C} + AB\bar{C}$

(c) (9 pts) Derive a simplified algebraic description for f. Justify each step (provide the name of the rule that you are using).

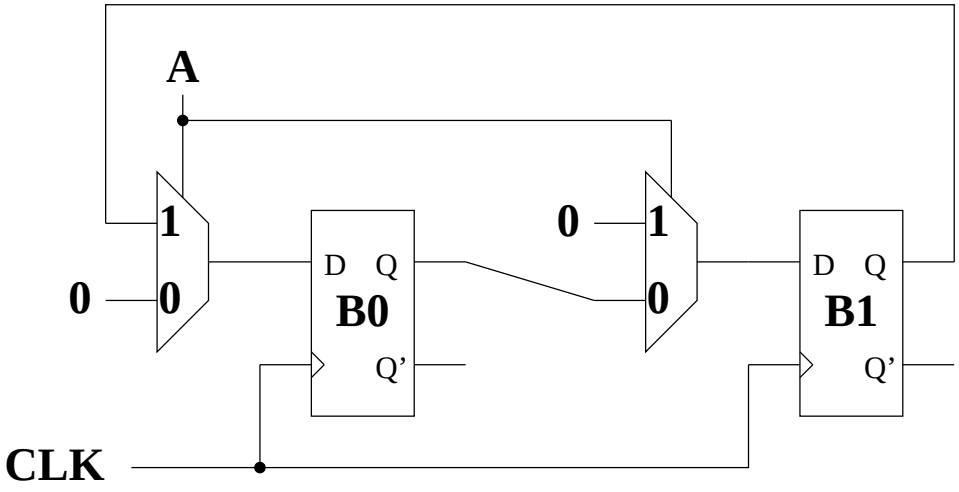
$\bar{A}B\bar{C} + AB\bar{C}$	
$(\bar{A} + A)B\bar{C}$	*Distributive Law*
$1 \times B\bar{C}$	$\bar{X} + X = 1$
$B\bar{C}$	$1 \times X = X$

(d) (5 pts) Draw the corresponding circuit.

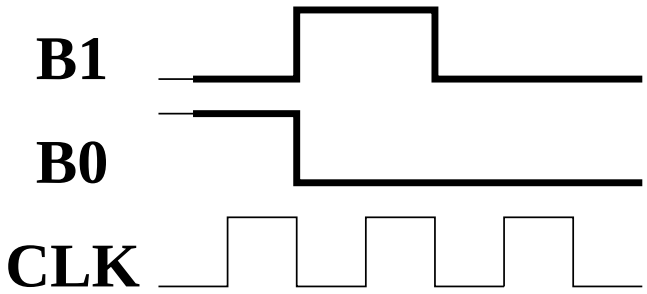


2. **Sequential Logic** (17 pts)

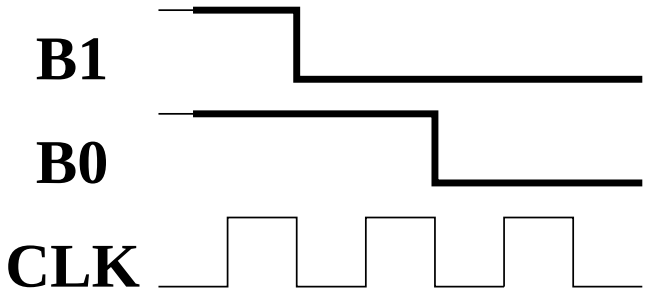
Given the following circuit:



(a) (6 pts) Assume that the initial state is $B1 = 0$ and $B0 = 1$, and that $A = 0$. Fill in the following timing diagram:



(b) (6 pts) Assume that the initial state is $B1 = 1$ and $B0 = 1$, and that $A = 1$. Fill in the following timing diagram:



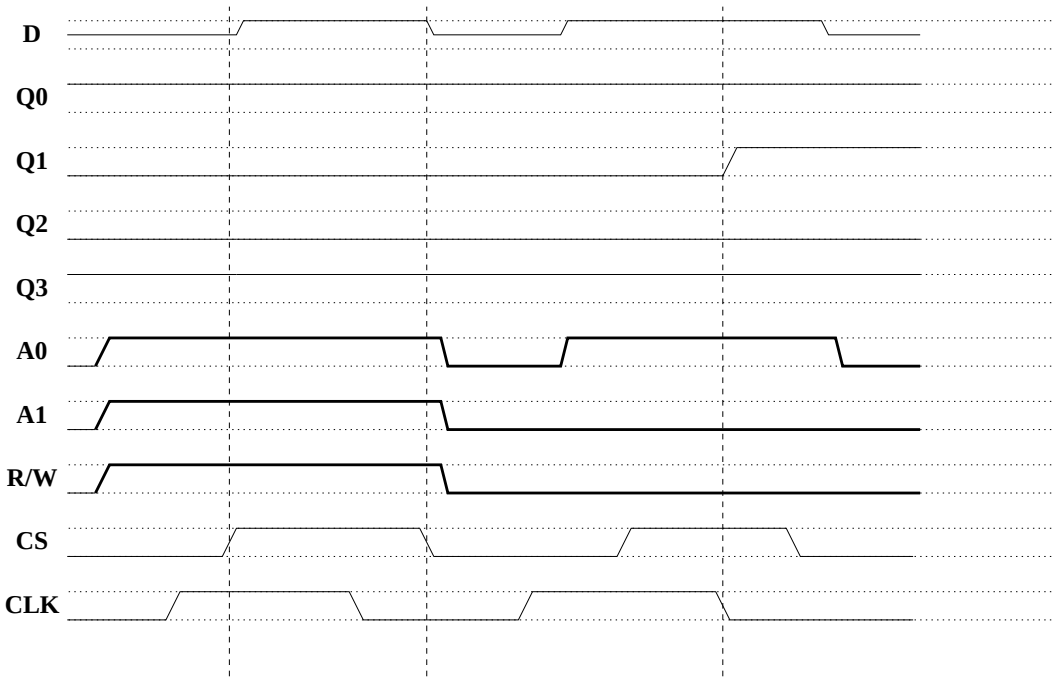
(c) (5 pts) If you interpret $B1, B0$ as a 2-bit number, what mathematical operation(s) does this device perform on each clock cycle?

When $A = 0$, the number is multiplied by 2 (carries are lost). OR: this is a register that shifts the bits left.

When $A = 1$, the number is divided by 2 (remainders are lost). OR: this is a register that shifts the bits right.

3. **Memory** (20 pts)

(a) (10 pts) For the timing diagram below, fill in the missing control signals. Specifically, we wish to read from $Q3$, and then write a 1 to $Q1$.

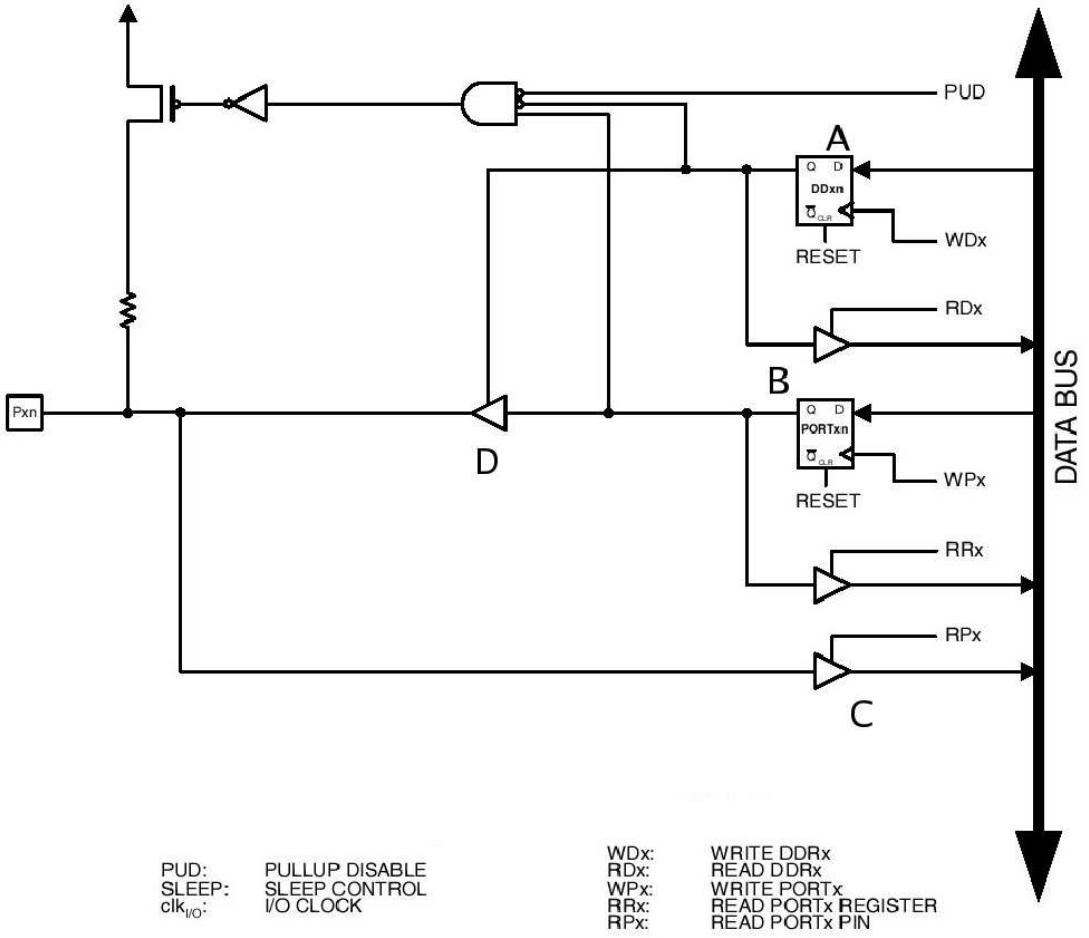


Note: we were pretty liberal about grading the timing diagram. In addition to having the signals be in the correct states (at certain times), we looked for having the signals be set up in time for the read or write operation. Specifically, the address and R/W lines needed to be configured before the chip select line went high.

(b) (5 pts) True/False and explain: The chip select is an output from the memory chip.
False. The chip select is an input that tells the memory chip when it is active.

(c) (5 pts) True/False and explain: The data bus is an input to the memory chip.
True, although it is only the case sometimes (other times, it acts as an output).

4. **Microcontrollers** (20 pts)



(a) (5 pts) Identify component "C". Briefly explain the function of this component in this circuit.

Component C is a tristate buffer. RPx is brought high on a read operation (e.g., foo = PINB;). When this happens, the state of the pin is used to drive the data bus. In all other cases, RPx is low and and the state of the pin does not have any influence on the data bus.

Assume an initial state of:
$DDRB = 0x36$
$PORTB = 0xA5$

(b) (5 pts) What effect does the following code have on $DDRB$ and on the above circuit (in terms of components A, B, C, and D)?

```
DDRB = DDRB & ~0x2;
```

This line of code ensures that bit 1 of DDRB is turned off (component A), but leaves the other bits of DDRB unchanged. In turn, this turns off the select line of component D, which will leave this pin floating.

(c) (5 pts) What effect does the following code have on the state of this circuit (in terms of components A, B, C, and D)?

```
PORTB = PORTB | 0x30;
```

This line of code ensures that bits 4 and 5 of PORTB are turned on (component B). However, in this case, only bit 4 changes state (bit 5 is already turned on).

(d) (5 pts) What is the function of the program counter? (be brief)
The program counter keeps track of which instruction is currently being executed.

5. **Timers** (16 pts)

(a) (8 pts) Given a system clock of $16MHz$ and a prescaler of 8. How long does it take for timer 0 to count from 0 to 200?
$\frac{200 \times 8}{16000000} = 0.1ms$

(b) (8 pts) Given a system clock of $16MHz$ and a prescaler of 64. How long does it take for timer 2 to count from 0 to 400?
Timer 2 cannot count to 400. So - we would be waiting forever.