Embedded Real-Time Systems (AME 3623)
Homework 2

February 11, 2010

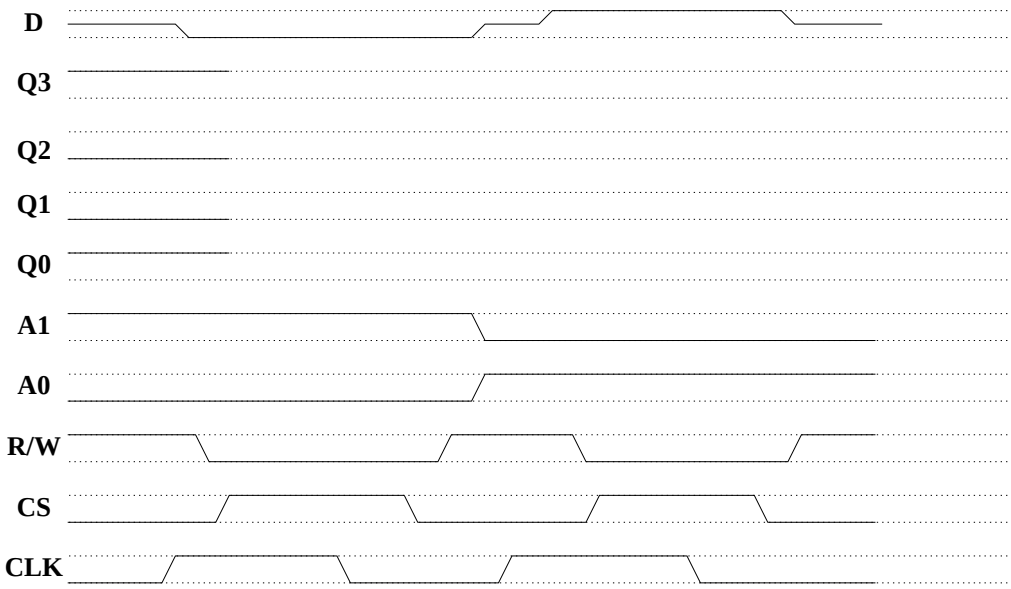
This homework assignment is due on Tuesday, February 16th in class (9:00 am). Your work may be handed in electronically (use the **Homework 2** digital dropbox on D2L), but please bring a hardcopy to class.

This assignment must be done individually: do not share/discuss your answers with others or look at the answers of others.

Question 1

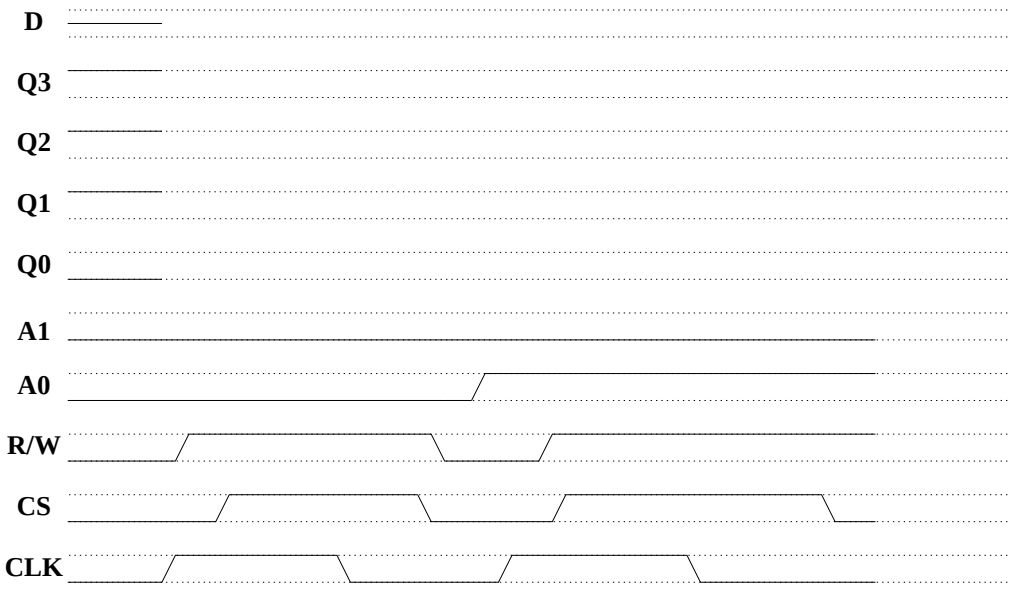
(10pts) Consider the four-element memory "chip" that we discussed in class (each element is "one bit wide"). Given the following timing diagram, fill in the missing traces ($Q0$, $Q1$, $Q2$, and $Q3$).

Hint: first re-examine the rules for writing to and reading from a memory chip.



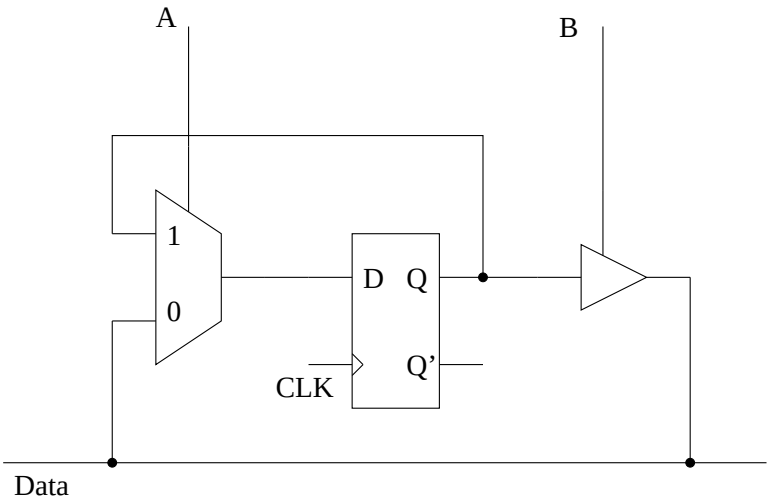
Question 2

(10pts) Consider the same four-element memory chip. Given the following timing diagram, fill in the missing traces (D, $Q0$, $Q1$, $Q2$, and $Q3$).



Question 3

The following circuit is a partial implementation of a 1-bit memory sitting on the data bus *Data*.



1. (10pts) Suppose that Q is initially set to 1. If $A = 1$, $B = 0$, $Data = 0$ and the clock transitions from high to low, what happens to Q and when?

2. (10pts) Suppose that Q is initially set to 1. If $A = 1$, $B = 1$ and the clock transitions from high to low, what happens to Q and $Data$, and when?

3. (10pts) Suppose that Q is initially set to 1. If $Data = 0$, $A = 0$, $B = 0$ and the clock transitions from high to low, what happens to Q, and when?

4. (10pts) Generally, what is the meaning of B?

5. (10pts) Assume memory control signals in the previous problems (CS, R/W, $A1$, and $A0$), and that this is memory element number 3 (counting from 0). Give the truth table for B. Note: the *Data* wire on this question corresponds to the lines labeled "D" on questions 1 and 2.

CS	R/W	$A1$	$A0$	B
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

6. (10pts) Design a circuit that implements B.

Question 5

How much time did you spend on this assignment?