Embedded Real-Time Systems (AME 3623)
Homework 2 Solutions

March 3, 2010

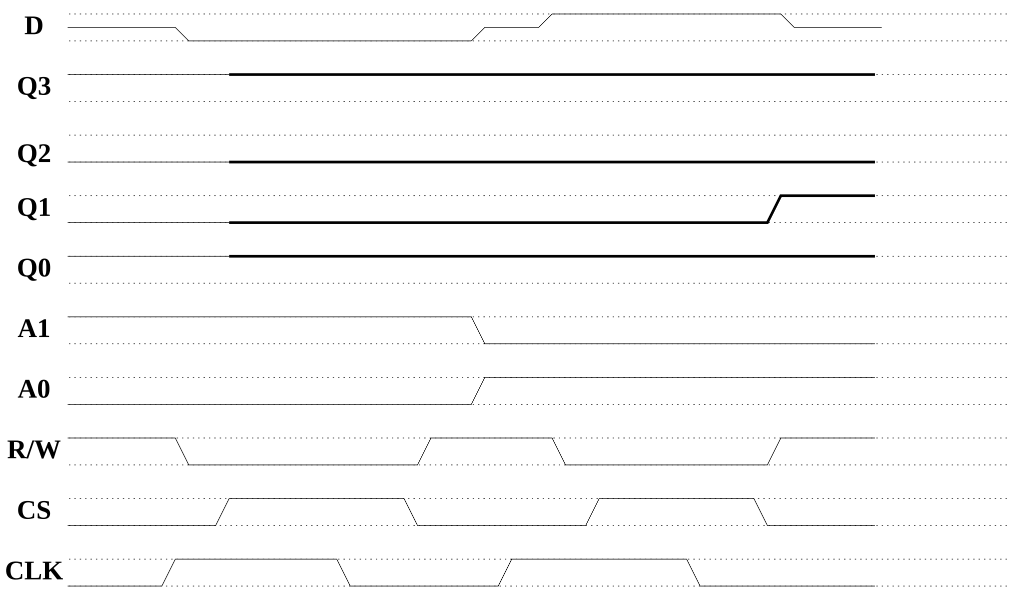
Question 1

(10pts) Consider the four-element memory "chip" that we discussed in class (each element is "one bit wide"). Given the following timing diagram, fill in the missing traces ($Q0$, $Q1$, $Q2$, and $Q3$).

Hint: first re-examine the rules for writing to and reading from a memory chip.

Both memory accesses are write operations; they affect the state of Q2 and Q1, respectively (but only when the clock transitions from high to low). However, the state of Q2 does not change since it already has a value of 0.

(answer is shown in bold)

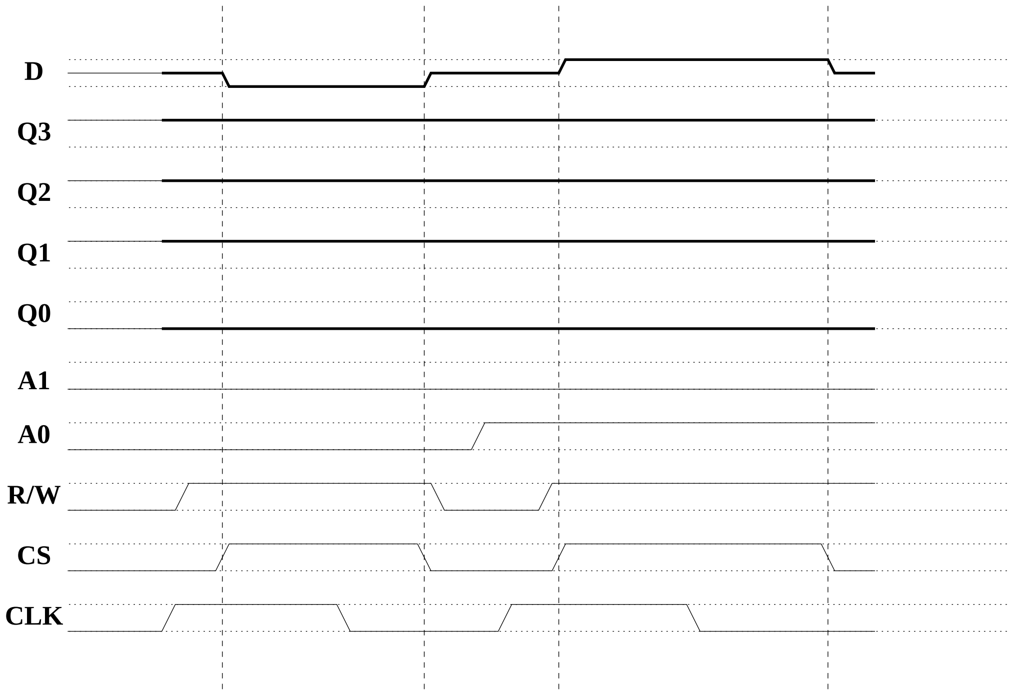


Question 2

(10pts) Consider the same four-element memory chip. Given the following timing diagram, fill in the missing traces (D, $Q0$, $Q1$, $Q2$, and $Q3$).

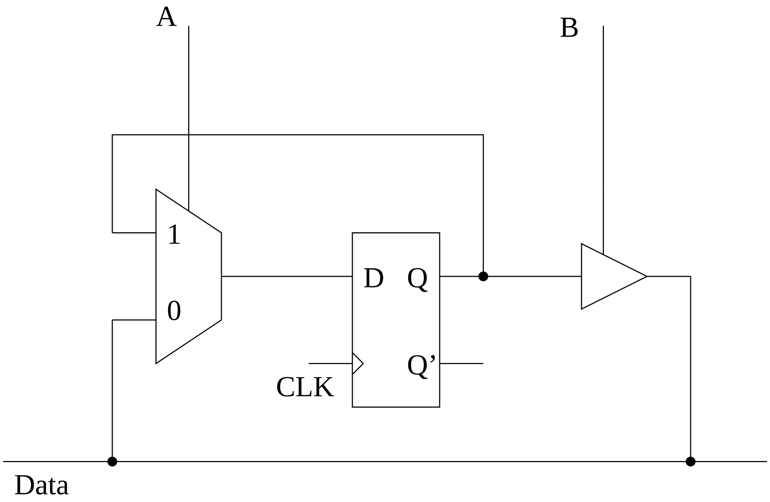
Both of these operations are read operations of elements Q0 and Q1. None of the memory elements change state. The data bus is driven during the entire time that the chip select line is high.

(answer is shown in bold)



Question 3

The following circuit is a partial implementation of a 1-bit memory sitting on the data bus *Data*.



1. (10pts) Suppose that Q is initially set to 1. If $A = 1$, $B = 0$, $Data = 0$ and the clock transitions from high to low, what happens to Q and when?

   Because the multiplexer is selecting the Q input (back to D), the flip-flop does not change state.

2. (10pts) Suppose that Q is initially set to 1. If $A = 1$, $B = 1$ and the clock transitions from high to low, what happens to Q and $Data$, and when?

   Because the multiplexer is selecting the Q input, then the flip-flop does not change state. $Data$ is driven to a state of 1 by the tristate buffer as long as $B = 1$.

3. (10pts) Suppose that Q is initially set to 1. If $Data = 0$, $A = 0$, $B = 0$ and the clock transitions from high to low, what happens to Q, and when?

   Because $A = 0$, $Data$ is selected as the input to the flip-flop. Therefore, when the clock changes from high to low, Q becomes 0

4. (10pts) Generally, what is the meaning of B?

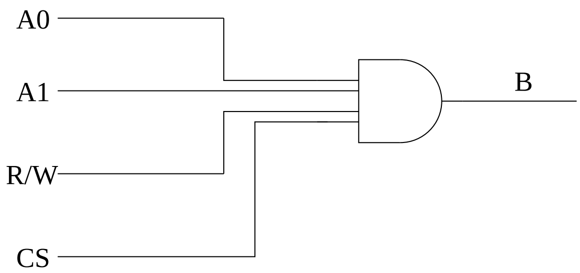
   When B is high, this memory element drives the bus. In other words: we are doing a **read** operation **from** the memory element.

5. (10pts) Assume memory control signals in the previous problems (CS, R/W, $A1$, and $A0$), and that this is memory element number 3 (counting from 0). Give the truth table for B. Note: the $Data$ wire on this question corresponds to the lines labeled "D" on questions 1 and 2.

   B is high when we are doing a read operation from element 3 of the 4-element memory. In order for this to occur, we must have: $CS = 1$, $R/W = 1$, and $A1, A0 = 11$. All other rows are zero, which indicates no driving of the data bus from our memory element.

CS	R/W	$A1$	$A0$	B
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

6. (10pts) Design a circuit that implements B.



(note: we will have a slightly different circuit for each of the other memory elements).